a pair of opposing spacers located above the adjacent pair of insulated wordlines, wherein the spacer isolate the buried bitline from the pair of storage node plugs.

12.(Amended) The [memory device] <u>integrated circuit</u> of claim 11, wherein the bitline plug includes polysilicon.

13.(Amended) The [memory device] <u>integrated circuit</u> of claim 11, wherein the pair of storage node plugs includes polysilicon.

14.(Amended) The [memory device] <u>integrated circuit</u> of claim 11, wherein the [memory device] <u>integrated circuit</u> further includes a pair of storage node contacts, wherein each of the storage node contact individually couples to one of storage node plugs.

15.(Amended) The [memory device] <u>integrated circuit</u> of claim 11, wherein the [memory device] <u>integrated circuit</u> includes a dynamic random access memory (DRAM).

16.(Amended) The [memory device] <u>integrated circuit</u> of claim 11, wherein the [memory device] <u>integrated circuit</u> includes a synchronous random access memory (SRAM).

17.(Amended) [A data handling system] <u>An integrated circuit</u>, comprising:

a central processing unit;

a [memory device] <u>storage unit</u>, wherein the [memory device] <u>storage unit</u> comprises:

multiple insulated wordlines having top surfaces, wherein the insulated wordlines are spaced apart from one another and formed on a substrate;

a bitline plug located between an adjacent pair of the insulated wordlines, the bitline plug having a top surface beneath the top surfaces of the insulated wordlines;

a pair of storage node plugs located on the opposite side of the adjacent wordlines from the bitline plug, wherein the pair of storage node plugs each have a top surface above the top surfaces of the insulated wordlines and are formed over portions of the adjacent wordlines;

a buried bitline coupled to the bitline plug; and

a pair of opposing spacers located above the pair of adjacent wordlines and isolating the buried bitline from the pair of storage node plugs; and

a system bus for communicatively coupling the central processing unit and the [memory device] <u>storage unit</u>.

18.(Amended) The [data handling system] <u>integrated circuit</u> of claim 17, wherein the bitline plug includes polysilicon.

19.(Amended) The [data handling system] <u>integrated circuit</u> of claim 17, wherein the pair of storage node plugs includes polysilicon.

20.(Amended) The [data handling system] <u>integrated circuit</u> of claim 17, wherein the [memory device] <u>storage unit</u> further includes a pair of storage node contacts, wherein each of the storage node contact individually couples to one of storage node plugs.

21.(Amended) The [data handling system] <u>integrated circuit</u> of claim 17, wherein the [memory device] <u>storage unit</u> includes a dynamic random access memory (DRAM).

22.(Amended) The [data handling system] <u>integrated circuit</u> of claim 17, wherein the [memory device] <u>storage unit</u> includes a synchronous random access memory (SRAM).

29.(Amended) A [data handling system] <u>integrated circuit</u> comprising:

a [central processing unit] <u>processor</u>; and

a [memory device] <u>storage unit</u> connected to the [central processing unit] <u>processor</u>, [memory device] <u>storage unit</u> including:

a number of semiconductor surface structures spaced apart along the substrate;

a number of plugs contacting the substrate between the number of surface structures, wherein the number of plugs includes an inner plug and a pair of outer plugs, each one of the outer plugs being formed adjacent to and on opposing sides of the inner plug, each one of the outer plugs having upper portions, wherein the upper portions cover top surfaces of the surface structures, wherein the inner plug is beneath the top surfaces of the surface structure; and

an inner electrical contact coupling to the inner plug and separated from the upper portions by a pair of opposing spacers.

30.(Amended) The [data handling system] <u>integrated circuit</u> of claim 29 further comprising a pair of outer contact regions, each being connected to one of the outer plugs.

31.(Amended) [A data handling system] <u>An integrated circuit</u> comprising:

a [central processing unit] <u>processor</u>; and

a [memory device] <u>storage unit</u> connected to the [central processing unit] <u>processor</u>, the [memory device] <u>storage unit</u> including:

first and a second surface structures, each having a top surface;

an inner plug located in between the first and second surface structures and beneath the top surface of each of the first and second surface structures;

a pair of outer plugs, each having an upper portion covered the top surface of one of the first and second surface structures;

an inner electrical contact connected to the inner plug; and

a pair of spacers for separating the inner plug and the inner electrical contact from the pair of outer plugs.

32.(Amended) The [data handling system] <u>integrated circuit</u> of claim 31 further comprising a pair of outer contact regions, each being connected to one of the outer plugs.

33.(Amended) The [data handling system] <u>integrated circuit</u> of claim 31, wherein the outer plugs are on opposing sides of the inner plug.

34.(Amended) The [data handling system] integrated circuit of claim 31, wherein the pair of spacers are located on opposing sides of the inner plug.

Claims 1-34 are now pending in this application. The Examiner is invited to contact Applicant's representative, Viet Tong, (612) 373-6969 with any questions regarding the present application.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 28th day of February, 2002.

Name Amy Moriarty Signature ______________________

Add'l Amnd Supp B
5-7-02

Docket No. 303.645US2
WD # 428085

Micron Ref. No. 98-0197.03

Clean Version of Pending Claims

METHOD AND STRUCTURE FOR IMPROVED ALIGNMENT TOLERANCE IN MULTIPLE, SINGULARIZED PLUGS
Applicant: Thomas A. Figura
Serial No.: 10/004,656

Claims 1-34, as of February 28, 2002 (date of supplemental preliminary amendment filed.).

1. An integrated circuit device on a substrate, comprising:

a number of semiconductor surface structures spaced apart along the substrate;

a number of plugs contacting the substrate between the number of surface structures, wherein the number of plugs includes an inner plug and a pair of outer plugs, each one of the outer pair being formed adjacent to and on opposing sides of the inner plug, each one of the outer pair having upper portions, wherein the upper portions cover areas of the surface structures; and

an inner electrical contact coupling to the inner plug and separated from the upper portions by a pair of opposing spacers.

2. The device of claim 1, wherein the device further includes a pair of outer contact regions, wherein each of the outer contacts individually couples to one of the outer pair of plugs.

3. The device of claim 2, wherein the pair of outer plugs include storage node plugs, and wherein the outer contact regions include storage nodes.

4. The device of claim 1, wherein the number of semiconductor surface structures includes isolated wordlines.

5. The device of claim 1, wherein the number of semiconductor surface structures includes isolated flash memory cells.

6. The device of claim 1, wherein the inner plug is formed beneath a top surface of the number of semiconductor surface structures.

7. The device of claim 1, wherein the number of plugs include polysilicon plugs.

8. The device of claim 1, wherein the inner plug includes a bitline plug, and wherein the inner electrical contact includes a bitline contact.

9. The device of claim 1, wherein the device includes a dynamic random access memory (DRAM).

10. The device of claim 1, wherein the device includes a synchronous random access memory (SRAM).

B1

11.(Amended) An integrated circuit, comprising:

multiple insulated wordlines having top surfaces, wherein the insulated wordlines are spaced apart from one another and formed on a substrate;

a bitline plug located between an adjacent pair of the insulated wordlines, the bitline plug having a top surface beneath the top surfaces of the insulated wordlines;

a pair of storage node plugs located on the opposite side of the adjacent pair of insulated wordlines from the bitline plug, wherein the pair of storage node plugs each have a top surface above the top surfaces of the insulated wordlines and are formed over portions of the adjacent wordlines;

a buried bitline coupled to the bitline plug; and

a pair of opposing spacers located above the adjacent pair of insulated wordlines, wherein the spacer isolate the buried bitline from the pair of storage node plugs.

B1 cont

12.(Amended) The integrated circuit of claim 11, wherein the bitline plug includes polysilicon.

13.(Amended) The integrated circuit of claim 11, wherein the pair of storage node plugs includes polysilicon.

14.(Amended) The integrated circuit of claim 11, wherein the integrated circuit further includes a pair of storage node contacts, wherein each of the storage node contact individually couples to one of storage node plugs.

15.(Amended) The integrated circuit of claim 11, wherein the integrated circuit includes a dynamic random access memory (DRAM).

16.(Amended) The integrated circuit of claim 11, wherein the integrated circuit includes a synchronous random access memory (SRAM).

17.(Amended) An integrated circuit, comprising:

a central processing unit;

a storage unit, wherein the storage unit comprises:

multiple insulated wordlines having top surfaces, wherein the insulated wordlines are spaced apart from one another and formed on a substrate;

a bitline plug located between an adjacent pair of the insulated wordlines, the bitline plug having a top surface beneath the top surfaces of the insulated wordlines;

a pair of storage node plugs located on the opposite side of the adjacent wordlines from the bitline plug, wherein the pair of storage node plugs each have a top surface above the top surfaces of the insulated wordlines and are formed over portions of the adjacent wordlines;

a buried bitline coupled to the bitline plug; and

a pair of opposing spacers located above the pair of adjacent wordlines and isolating the buried bitline from the pair of storage node plugs; and

a system bus for communicatively coupling the central processing unit and the storage unit.

B1 cont

18.(Amended) The integrated circuit of claim 17, wherein the bitline plug includes polysilicon.

19.(Amended) The integrated circuit of claim 17, wherein the pair of storage node plugs includes polysilicon.

20.(Amended) The integrated circuit of claim 17, wherein the storage unit further includes a pair of storage node contacts, wherein each of the storage node contact individually couples to one of storage node plugs.

21.(Amended) The integrated circuit of claim 17, wherein the storage unit includes a dynamic random access memory (DRAM).

22.(Amended) The integrated circuit of claim 17, wherein the storage unit includes a synchronous random access memory (SRAM).

23. An integrated circuit device comprising:

first and a second surface structures, each having a top surface;

an inner plug located in between the first and second surface structures and beneath the top surface of each of the first and second surface structures;

a pair of outer plugs, each having an upper portion covered the top surface of one of the first and second surface structures;

an inner electrical contact connected to the inner plug; and

a pair of spacers for separating the inner plug and the inner electrical contact from the pair of outer plugs.

24. The integrated circuit device of claim 23 further comprising a substrate connected to the first and second surface structures, the inner plug, and the pair of outer plugs.

25. The integrated circuit device of claim 24, wherein the first and second surface structures are spaced apart along the substrate.

26. The integrated circuit device of claim 23 further comprising a pair of outer contact regions, each being connected to one of the outer plugs.

27. The integrated circuit device of claim 23, wherein the outer plugs are on opposing sides of the inner plug.

28. The integrated circuit device of claim 23, wherein the pair of spacers are located on opposing sides of the inner plug.

B2

Sub C2

29.(Amended) A integrated circuit comprising:

a processor; and

a storage unit connected to the processor, storage unit including:

a number of semiconductor surface structures spaced apart along the substrate;

a number of plugs contacting the substrate between the number of surface structures, wherein the number of plugs includes an inner plug and a pair of outer plugs, each one of the outer plugs being formed adjacent to and on opposing sides of the inner plug, each one of the outer plugs having upper portions, wherein the upper portions cover top surfaces of the

B2 Cont

surface structures, wherein the inner plug is beneath the top surfaces of the surface structure; and

an inner electrical contact coupling to the inner plug and separated from the upper portions by a pair of opposing spacers.

30.(Amended) The integrated circuit of claim 29 further comprising a pair of outer contact regions, each being connected to one of the outer plugs.

31.(Amended) An integrated circuit comprising:

a processor; and

a storage unit connected to the processor, the storage unit including:

first and a second surface structures, each having a top surface;

an inner plug located in between the first and second surface structures and beneath the top surface of each of the first and second surface structures;

a pair of outer plugs, each having an upper portion covered the top surface of one of the first and second surface structures;

an inner electrical contact connected to the inner plug; and

a pair of spacers for separating the inner plug and the inner electrical contact from the pair of outer plugs.

32.(Amended) The integrated circuit of claim 31 further comprising a pair of outer contact regions, each being connected to one of the outer plugs.

33.(Amended) The integrated circuit of claim 31, wherein the outer plugs are on opposing sides of the inner plug.

34.(Amended) The integrated circuit of claim 31, wherein the pair of spacers are located on opposing sides of the inner plug.